10th International Electrostatic Discharge Workshop
IEW

ESD ASSOCIATION ®

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Evangelische Akademie Tutzing, Germany

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A highly rewarding experience!

The International ESD Workshop (IEW) hosts its 10th annual event at the majestic Evangelische Akademie, Tutzing, Germany. The IEW provides the perfect opportunity for participants to meet in a relaxed, invigorating atmosphere and engage in discussions about the latest research and issues of interest within the EOS/ESD community.

IEW facilitates access to and interactions with industry leaders through invited seminars, technical sessions, special interest groups (SIGs), discussion groups (DGs), and invited speakers. This year we focus on Automotive applications EOS/ESD/EMC, ESD co-design

Experience the uniquely interactive program of the IEW Workshop.
• Listen to viewpoints of industry experts
• Share your ideas and opinions on EOS/ESD topics
• Explore industry best practices and give your inputs
• Interact and network with high-level EOS/ESD industry experts

This Workshop is a highly rewarding and engaging experience for all! Whether you are new to EOS/ESD topics, or an old hand at it - join us at IEW 2016 to learn in an informal, interactive, and engaging atmosphere.

IEW 2010 Poster Session, Evangelische Akademie, Tutzing, Germany

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Joost Willemen, Infineon Technologies

EXPERIENCE IEW

Welcome to the 10th annual International ESD Workshop (IEW). This important event offers the unique opportunity to learn and discuss technical issues on EOS and ESD topics in an informal and friendly environment, encouraging extensive interactions among all attendees.

Located on the shores of Lake Starnberg, 40 kilometers southwest of Munich, lies the Tutzing estate and its 18th century mansion. With modern conference rooms and facilities, this venue is well suited for the workshop. The on-site single and double bedrooms provide a comfortable stay within the quietness of the private park around the castle. From the balconies and the patios there is a magnificent view of the Bavarian Alps. The spirit of this location encourages thoughtful discussion and intensive interaction.

Scheduled poster sessions form the core of the technical program. These poster sessions are preceded by a brief introduction of each poster by the authors in a plenary "teaser" session. These teasers encourage the participants to select the posters of greatest interest for the poster discussion sessions. Meet and chat with the authors, while you expand your knowledge and network in the subsequent poster discussion session. To compliment the offering attendees are also encouraged to bring open posters. This format provides an ideal forum for learning and interchange of new ideas. Topics covered in the poster sessions include IC EOS/ESD design, verification, test, multichip, and system level ESD.

The Discussion Groups (DGs) held in the evenings are a unique part of our interactive workshop. While each EOS/ESD topic discussion is facilitated by an expert on the subject, the main discussion will take place among the DG participants. The discussion groups will address topics of the focus issues and include 3D-IC, AEC Q-100 target levels, ESD foundry and IP vendor parameters, on-chip ESD robust design in smart power technologies and other interesting topics. The IEW also provides a similar forum for Special Interest Groups (SIGs), on selected subjects that may extend beyond the IEW time frame. Some SIGs have been successfully meeting for several years.

A number of stimulating state-of-the-art EOS/ESD seminars, as well as invited talks are scheduled. Come and listen to presentations discussing self-driving cars, contact CDM and CC-TLP methods, EOS/ESD challenges in LED lighting, and other exciting topics.

As a break to EOS/ESD discussions, and to provide an opportunity to enjoy the spectacular surroundings, an afternoon is reserved for recreation with fellow attendees. This is a great way to become better acquainted with your EOS/ESD colleagues.

Come and meet experts, share your views, ask questions, and extend your network with EOS/ESD experts from industry and academia. Above all, learn how to efficiently deal with today's EOS/ESD challenges and prepare for tomorrow in an informal and interactive atmosphere. Register for this event early. This will help us in the final planning and preparation for a highly successful event. We sincerely hope that you will join us in Tutzing for the 2016 IEW.

Photos: IEW 2010,
Evangelische Akademie, Tutzing, Germany

IEW 2015 Poster Session

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MONDAY EVENING

Bavarian Evening: IEW welcomes travelers from abroad and local guests on Monday, May 16 with a colorful program of Bavarian traditions ranging from an archetype of communication 'Jodeln' to a particular form of dancing 'Schuhplattln'. Join and meet your friends and peers in a relaxed atmosphere.

KEYNOTE
Keynote Speaker Chair: Christoph Thienel, Robert Bosch, GmbH

Robustness Challenges for Technologies 28nm and below in Automotive Environment

Jürgen Weyer, NXP Semiconductors

Jürgen Weyer

The use of deep submicron technologies is challenging especially for automotive temperature and lifetime profiles.

To name a few of them:

- The FinFet technology (≤16nm) is no longer a planar two-dimensional technology, it is a three dimensional technology that needs mechanical stress in a further direction to be covered.

- On each CMOS gate on a few 10s of electrons make a difference between the on/off state, any kind of very small leakage can be disastrous.

- Local heating at transistor level is a factor which requires careful design techniques including the addition of "cooling metals". Missing these design techniques can lead to long term reliability problems.

- The lower metal connections are very thin and small, thus increasing, in combination with the local heating the risk of electromigration fails.

- The ESD & EOS robustness of the transistors is reduced due to thin oxides, and short channel length. Increasing the die area to be able to take more energy is commercially not viable.

Given that potential solutions beyond chip-level are required – external protections – architectures.

Some of them will be shown and discussed as part of this presentation.

Biography:

Description of Current Responsibility

• Vice president Automotive Sales – EMEA

• Managing director – Freescale Halbleiter Deutschland - GmbH

Professional Experience

Motorola:

• 1980: Product marketing engineer for logic ICs; positions of increasing responsibility in the areas of marketing, operations and sales.

• 1987 to 1992: Product marketing manager for ASICs.

• 1992: Relocation to Toulouse as operations manager, MOS Digital Analog Division (MDAD); managing of the Wireless Operation with the Communications and Advanced Consumer Technologies Group (CACTG); moving on to become operations manager for Global Systems for Mobile Communications (GSM) within the Wireless Subscriber Systems Group.

• 1998: Director of global sales for the Transportation Systems Group EMEA/Asia-Pac.

• 2003: General manager Automotive Sales & Marketing – EMEA

• 2006: Vice president Automotive Sales and Marketing – EMEA

Freescale:

• 2004: Vice president Automotive Sales and Marketing – EMEA

NXP:

• 2015 Vice president Automotive Sales – EMEA

Education

• Studied electronics at the Fachhochschule Coburg where he obtained his degree.

INVITED TALKS

Invited Speaker Co-Chairs:
Michael Mayerhofer, Infineon Technologies
Lorenzo Cerati, STMicroelectronics

Invited talks are one of the key elements of the workshop, featuring the theme of the workshop as well as focusing on some advanced topics of interest. There are four invited talks this year. Industry leaders and experts from Infineon, Intel, and Audi will share their thoughts on topics regarding recent trends in ESD protection devices, automotive semiconductors, and EOS in the invited talks.

Invited Talk 1

ESD Protection Devices and Technologies: Recent Advances and Trends

Werner Simbürger, Matteo Rigato, Clement Fleury, Dionyz Pogany, Joost Willemen, Vadim Vendt, Thomas Schwingshackl, Antoine D'Arbonneau, Infineon

Abstract: Transient voltage suppressors (TVS) are widely used for electrostatic discharge (ESD) and surge protection of electronic devices. Especially the application of mobile devices for wireless communications requiring extremely high production quantities in the range of multi-billion pieces of TVS per year. The very small size of the TVS, e.g. 0.4 mm x 0.2 mm x 0.15 mm, and the high production quantities require new process and packaging technologies.

Self-protection of devices in advanced CMOS and bipolar technologies is a key feature for RF applications in order not to degrade the RF performance by additional protection devices.

This presentation discusses the key performance parameters, failure analysis, and characterization methods of different technologies with low parasitic capacitance in the picoFarad and sub-picoFarad range.

Biography: Werner Simbürger received a PhD degree in electrical engineering from Vienna University of Technology, Austria, in 1995. From 1995 to 1999 he was with Siemens AG in Munich, Germany, as a RF design engineer working on integrated power amplifiers. From 1999 to 2005 he joined Infineon Corporate Research as department head for integrated RF circuit design. In the time from 2005 to 2007 he was responsible for the CMOS power amplifier SoC design (DECT) at the Infineon Wireless product division. Since 2007 he has been responsible for RF and ESD R&D at various divisions of Infineon. In 2009, He was co-founder of the company "High Power Pulse Instruments (HPPI) GmbH" in Munich.

Invited Talk 2

Road to Self Driving Cars – View of a Semiconductor Supplier

Hans Adlkofer, Infineon Automotive System

Abstract: 40 years ago there were nearly NO semiconductors in cars. Besides a generator, supplying power for lighting, ignition, and simple relays and switches, the car was a pure mechanical system. Today, the car is dominated by electronics and 80% of the innovation happening in the car is based on semiconductors.

We stand on the border towards e-mobility, advanced driver assistant system, connected cars and despite 80 million produced cars per year we have the lowest level of dead people on the road. On the other hand, the amount of cars, specifically in the fast growing mega cities, will require more modern mobility concepts which will have also a strong impact on the car industry.

Looking 40 years down the road, we will see many more mega cities, people online 24 hours a day, and the workplace will be around the world and at home. This will have also a major impact on the use of cars. Mega cities cannot handle all the traffic with private cars, therefore integration of mobility concepts will be key for the city planners to avoid constant traffic jams, air pollution, parking space problems, and to achieve convenient and efficient mobility. Flexible and integrated mobility concepts will push topics like car sharing, autonomous driving, connected car concepts, and new types/setups of cars; including 3 wheelers to small cars driving in a convoy.

The semiconductor industry will be challenged to support increasing and new requirements to enable self-driving by providing semiconductors with high computing power, high speed networks, and redundant features to get functional safe operational systems. This will take several steps of learning, system optimization and new technology in automotive semiconductor not used today in the industry. That means consumer technology made ready for automotive or new technologies fulfilling automotive requirements.

Functional safety, cyber security, and energy on demand will reorganize the vehicle electronic architecture and partitioning. Domain control will become standard with major backbone communication between domains. Vehicles will be connected to other vehicles as well as the infrastructure.

Biography: Hans Adlkofer studied electronics with a focus on semiconductor technologies. He started his career at National Semiconductor in the marketing department with focus on ASICs for the automotive industry.

The next career step was at Giesecke & Devrient to develop secure operating systems for smart cards. Thereafter, he moved on to SIEMENS Semiconductor (today Infineon) where he headed an application center for security and smart card ICs. Later, he moved to Singapore to head the business operation for the Asian market.

In 2003, he took over the responsibility for the sensors business unit in Infineon Technologies. Since 2009, he is heading the System Group Activities in the automotive division of Infineon.

Invited Talk 3

View from a Leading Car Manufacturer for Semiconductor Requirements Supporting Upcoming Automotive Requirements

Ulrich Abelein, AUDI

Abstract: The field of automotive electronics went through an impressive change over the last 20 years. Starting from a purely mechanical system with some electric parts, a modern vehicle turned into one of the most complex mobile electronic devices used today in our modern society. Electronics made cars safer, greener, more comfortable, and easier to handle. Most innovations we have seen in vehicles over the last decade were either directly or indirectly enabled by electronics.

This development lead to completely new challenges for the automobile industry. Electronics knowledge became a core competence for a car maker and semiconductors have a essential influence on overall quality targets. Treating innovation and quality as a unity is therefore absolutely necessary for the use of state-of-the-art technologies in automotive applications.

This talk will give an overview of the special demands of a car manufacturer concerning electronics development, quality, and reliability. It will point out the influence of the automobile boundary conditions on the supply chain from the vehicle to the wafer. In this context some new approaches to deal with the upcoming challenges in this field will be sketched.

Biography: Ulrich Abelein is responsible for semiconductor quality and failure analysis within the AUDI AG. His responsibilities include the Audi semiconductor failure analysis lab and the strategic development of the fields of qualification and quality strategies for automotive semiconductors as well. He studied microelectronics and economics at the Technical University of Munich and the University of Hagen respectively.

In 2003, he joined the group of Prof. Eisele at the University of the Federal Armed Forces in Neubiberg/Munich. There he worked in the field of novel device concepts on silicon and process technology development. In 2008, he took over his current position at AUDI AG.

Invited Talk 4

Electrical Overstress (EOS) – Developing a Common Language and Understanding

Brett Carn, Harald Gossner, Intel

Abstract: Electrical overstress damage has been a leading cause of product returns for many, many years. The Industry Council has been working over the past several years to publish a white paper (WP) on EOS and has plans to publish this document in the second quarter of 2016. In this talk, we will discuss some of the key points in the WP. This will include an overview of the survey that was conducted as a part of preparing the WP, discussing a common language necessary in order to better understand EOS and its attributes, review some common root causes, and the approach needed in order to get to a true root cause. A case study will be reviewed in order to depict this approach. Finally, we will wrap up with a discussion on opportunities to minimize EOS in the future through cooperation.

Biography: Brett Carn initially joined Intel Corporation in 1999 and is a principal engineer in the Corporate Quality Network. He has actively worked in the field of device level ESD at Intel. In that role, Brett chairs the Intel ESD Council overseeing component level ESD and latchup testing across all Intel sites worldwide; defining all internal test specifications, reviewing all Intel ESD design rules, overseeing/defining the ESD target levels for all Intel products worldwide, and leading post silicon ESD debug on many products. In more recent years, Brett has also been actively involved with addressing EOS challenges at Intel. Since 2007, Brett has been a member of the Industry Council on ESD Target Levels and has helped author several whitepapers. Brett is an active member of the ESDA and a current member of the ESDA Board of Directors. Brett is also a member of the ESDA Education Council, a member of the Technical and Advisory Support Committee (TAS) and a member of the Joint WGs on HBM and CDM. Brett received his BS in electrical engineering from Portland State University in 1986.

Biography: Harald Gossner is senior principal engineer at Intel. In the 20 years of his career in ESD protection design he has authored and co-authored more than 100 technical papers and two books. He holds 60 patents on ESD protection and novel devices. For his contributions he received the best paper award of EOS/ESD Symposium in 2005 and 2012, as well as ESDA Outstanding Contribution Award in 2015. He has served in technical program committees of IEDM, EOS/ESD Symposium, and International ESD Workshops and is a member of the board of directors of EOS/ESD Association. In 2006, he became co-founder and co-chair of the Industry Council on ESD Target Levels, which will be publishing a white paper on EOS.

SEMINARS

Seminar Chair: Mirko Scholz, imec

We have four seminars this year which cover very diverse areas. The first seminar provides an overview on the analysis of ESD testing induced failures. Technology scaling makes failure analysis a more and more challenging task. A combination of electrical failure analysis and material characterization is required to identify the source and location of a failure. Several real case examples are used to illustrate the different analysis techniques. The second seminar covers an important ESD testing topic which is contact CDM. There are two main techniques, contact CDM and capacitive-coupled (CC) TLP, which are introduced in this seminar. The merits and limitations of each method are discussed also with respect to the existing CDM testing standards. The third seminar covers a topic which attracts more and more attention. Light Emitting Diodes (LED) opened huge opportunities for solid state lighting (SSL). This also bring new reliability challenges for the SSL manufacturers which are discussed from an EOS/ESD point of view. The forth seminar tries to link the two worlds of ESD control and ESD protection design. Practical tips on ESD control are provided together with the implementation of a comprehensive ESD control program. Real world examples show the increased ESD risk due to the charged board event, surprising damages due to hand tools, and how to identify ESD threats.

Seminar 1
Analysis of ESD Testing Induced Failures

Yong-Fen Hsieh, Materials Analysis Technology, Inc. (MA-tek)

Abstract: Driven by process technology scaling down, ESD zapping induced device failure is NOT easily found by optical microscope or SEM based observations. With the aids of electrical failure analysis and materials characterization techniques, various kind of critical failures were identified clearly, either on the surface of Si surface or buried in Si crystal lattice. Owing to limited capability of single diagnostic tool and complexity of device architecture in vertical scale, a combination of a variety of tools is known to be a must for root cause identification, in order to reach the ultimate performance of fault isolation and image resolution. Major contents of this lecture will cover many interesting examples of real cases, especially using TEM as a major tool for failure analysis.

Biography: Dr. Hsieh received her BS, MS, and PhD degrees of materials science and engineering from National Tsing-Hua University in Taiwan in 1981, 1983, and 1988, respectively. Her major interest of academic research was mainly focused on the metal contact formation on semiconductors.

Dr. Hsieh extended her professional interests to versatile materials systems when doing her postdoctoral research at AT&T Bell Labs, Murray Hill, NJ. During that time (1989-1991), she had been working with many research groups and published many papers on Cobalt implanted silicide formation, AlGaAs/GaAs surface emitting lasers, GaSb/InSb/GaSb laser diode, Si-Ge heterojunction bipolar transistors, YBCO/LaAlO3 superconductors, and FeSi3/GaAs metal contact formation. She also partially supported the physical analysis of the process development team of 4Mb SRAM in Allentown, PA; which upgraded her skills, not only in the fundamental studies, but also in the technology development of IC devices and products.

Dr. Hsieh joined the Taiwanese government sponsored research organization, ITRI, after finishing her academic researches. She was associated with MRL, working on the AlGaAs super-high brightness LED project and with ERSO as integration engineer of BiCMOS and 16Mb DRAM projects. It elucidated her ability to conduct an up-to-date industrial TD project from a scientific perspective.

In 1994, Dr. Hsieh commenced her career in industry. She was associated with UMC, IC Wafer Foundry, as the department heads of materials analysis, failure analysis, and quality assurance in the QRA division. In 2000-2001, after a inter-group companies transfer, she headed the Quality Management Division of Unipac Optoelectronic Corp., the first TFT-LCD Manufacturer in Taiwan. She was in charge of the operation of LCOS(Liquid Crystal on Si) Business Division after the merge of AU Optronics (ADT and Unipac).

In August 2002, with the wide knowledge base in research, integration, FA, and QRA in various industries, Dr. Hsieh decided to make every endeavor to contribute to the community by running an analytical lab, MA-tek. The company owns seven labs in Taiwan, Shanghai/China, and one sales office in Osaka/Japan and is known to be the first tier materials analysis lab worldwide. In 2006, it was elected to be a fast growth company in top 50/Taiwan and top 500/Asia by Delloitte. In 2008, it was the ONLY service lab awarded as the industrial excellence by Economy ministry of Taiwan. It was also formally listed in Taiwan stock market (No.3587) on Aug.18, 2009. In Jan. 2013, MA-tek was elected to be A+ enterprise by Global Views Monthly (遠見雜誌). It's business performance has been well recognized locally and globally.

Seminar 2
Advances in Contact CDM and CC-TLP Methods

Nathan Jack, Intel Corporation; Horst Gieser, Fraunhofer EMFT

Abstract: As package bump pitches shrink and protection design windows decrease, as well as the demand to test at wafer and die level, the inefficiencies and artifacts of FICDM testing necessitate innovation in CDM test methods. In the past decade, two major relay-based contact CDM (CCDM) test methods have been proposed as alternatives to field-induced CDM (FICDM). In this talk, low-impedance CCDM and capacitive coupled TLP (CCTLP) will be discussed. The merits and limits of each will be discussed, along with recent data showing correlation with the legacy FICDM tester. Thoughts on methods for inclusion in future standards and benchmarks will be presented.

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Biographies:
Nathan Jack received a BS in electrical and computer engineering from Utah State University, Logan, in 2007 and MS and PhD degrees in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, in 2009 and 2012, respectively.

Since 2012, he has been with Intel Corp. in Oregon as an ESD/LU Reliability Engineer. While a student, he completed a total of seven summer internships at Intel Corp., IBM, and Micron Technology, five of which were in the ESD/latchup R&D reliability groups. His research interests include on-chip ESD protection and ESD test methods.

Dr. Jack was the recipient of an Intel PhD fellowship for the 2011-2012 academic year. He was also the recipient of the Outstanding Paper Award and Best Student Paper Award from the 2011 EOS/ESD Symposium, and the Best Poster Award from IRPS. He has served as a technical session chair for the ESD Symposium, A/V co-chair for IEW, and a technical committee member for IRPS.

Dr.-Ing. Horst A. Gieser is head of the ATIS (Analysis and Test of Integrated Systems) team at the Fraunhofer-Institution for Microsystems and Solid State Technologies EMFT (www.emft.fraunhofer.de). He has received his diploma in electrical engineering and his PhD from the Technical University in Munich. He has authored and contributed to more than 65 publications. Four papers in the field of electrostatic discharge (ESD) won awards at international conferences. He is past-chair of the ESD FORUM e.V., the German non-profit ESD association furthering the exchange of scientific and professional experience. He has served the standardization of ESD-test methods and organized several international conferences and workshops. Beyond CC-TLP, CDM, and system level ESD his scientific interests are in the field of sensors, reliability, failure analysis of devices, circuits, and systems, as well as characterization techniques with ultra-short transients. He was also involved in lateral and vertical integration of modules and systems up to developing large area smart LED illumination in the i-Tex project.

Seminar 3
EOS/ESD Challenges in LED Lighting

Alessio Griffoni, OSRAM

Abstract: Advances in light emitting diode (LED) performance and cost, combined with the push for greater lighting efficiency and reliability, have created an unprecedented opportunity for solid state lighting (SSL). However, the manufacture of SSL systems can be far more complex than producers of traditional lighting are accustomed. On one hand, SSL is bringing new processes and materials into a commercial business as old as 150 years leading to new design concepts and challenges. On the other hand, the lighting industry is moving from offering a disposable product into a business that is selling high reliability products, e.g. up to 10 years of service. Hence, reliability and EOS/ESD robustness are key elements for SSL.

Biography: Alessio Griffoni received a BS in information engineering, a MS in electronic engineering, and a PhD in information science and technology from the University of Padova, Padova, Italy, in 2004, 2006, and 2010, respectively.

From 2008 until 2011, he was with imec, Leuven, Belgium, as researcher working on the ESD protection and radiation effects of advanced CMOS and HV technologies. Since 2011, he has been with OSRAM, Treviso, Italy, as senior R&D engineer working on the development and reliability of novel LED module concepts and products. Since 2015, he has led the EOS/ESD Association working group on EOS/ESD in LED lighting.

Dr. Griffoni has been a senior member of IEEE and ASQ since 2015. He is also a peer reviewer of the several IEEE and Elsevier journals and he has served in the TPC of the 2016 Accelerated Stress Testing and Reliability (ASTR) Conference; the 2016, 2015, and 2011 European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF); and the 2010 EOS/ESD Symposium.

Seminar 4

The Design Engineer: Weak link or Warrior in the ESD Battle?

Ginger Hansel, Dangelmayer Associates

Abstract: Design engineers strive to incorporate ESD protection into chip designs, but they are often unclear about the best way to handle the physical devices. The Industry Council on ESD Target levels documented a need to lower both the HBM and CDM thresholds with the confidence that factories already had the appropriate ESD control programs in place. However, many engineering labs do not understand or follow industry ESD guidelines and are unaware of the potential jeopardy created by these lower thresholds. Anyone doing device testing, characterization, TLP stress testing, board level analysis or upgrading their own computer should know basic ESD control techniques. This seminar will include practical ESD control tips for engineering labs, as well as how to set up and monitor a comprehensive ESD control program. Real world examples will show the increased ESD risk of Charged Board Events (CBE), the surprising damage due to hand tools, and how to use event detectors to identify ESD threats. You've spent a lot of effort doing careful designs – now take good care of your valuable test chips and prototype engineering samples.

Biography: Ginger Hansel joined Motorola's Semiconductor Products Sector in 1981 as a test process/equipment engineer to analyze and improve manufacturing operations. She founded and led the manufacturing ESD control team that trained, audited, qualified materials, and established innovative solutions throughout the semiconductor sector. Under her leadership, the team reduced a 40% failure rate in one test operation to almost zero through the targeted introduction of specific ESD control materials and ESD awareness training. Ginger brought ESD awareness to her other roles as engineering section leader, technical training manager, QA engineer, business metrics engineer, data and document control manager, program manager and technical product marketing manager. Ginger retired from Motorola/Freescale in 2004 and became director of marketing and program management with the ESD consulting group, Dangelmayer Associates.

She has published numerous magazine articles and technical papers on effective ESD control programs and awareness training; examples include "The Production Operator: Weak Link or Warrior in the ESD Battle" and "Cost Effective Failure Analysis Method for Detecting Failure Site Associated with Extremely Small Leakage". She has taught seminars, workshops, and webinars around the country and abroad. For over 35 years, Ginger has held leadership positions in the EOS/ESD Association such as president, board of directors, chair of the education business unit, and has served on the steering, technical program, standards, and other committees. She is currently the senior vice president of the EOS/ESD Association and chair of the services business unit group.

Ginger initiated the iNARTE ESD certification in 1992, and is a certified ESD control engineer. She is currently on the board of directors for the Texas ESD Association. Ms. Hansel received a BS in natural sciences (Psychology) and a BS in electrical engineering technology, both from the University of Houston. She received her MBA (Executive Option II program) from the University of Texas.

IEW 2015

DISCUSSION/SPECIAL INTEREST GROUPS

Discussion/Special Interest Groups Co-Chairs:
Christian Russ, Intel, christian.cornelius.russ@intel.com
Patrice Besse, Freescale Semiconductor, patrice.besse@freescale.com

The discussion groups are an integral part of the workshop. Parallel discussion groups are offered each evening on Tuesday and Wednesday. Each discussion group has one or two moderators with extensive expertise on the topic to help guide and inspire the discussion. The success of these sessions depends on your active participation. We encourage you to bring along data, ideas, and other items of interest to share. Contacting session moderators with questions, comments, or suggestions prior to the event is also encouraged. As the workshop approaches, please check the IEW web site for updates from the discussion group moderators. Interested in forming a new Special Interest Group (SIGs), focused on one compelling topic of mutual interest? Please contact Christian Russ or Patrice Besse for SIG creation details.

Discussion Groups Session A

DG A1: ESD Reliability in 3D Integration Technologies
Moderator: Mirko Scholz, imec
mirko.scholz@imec.be

3D integration is a very promising option for further effective scaling of integrated circuits (IC). It enables both higher integration density and heterogeneous integration thereby providing more functionality per foot print. Since 2014, a working group is meeting at ESDA events like the IEW and the Symposium to exchange/discuss the latest R&D results on the topic. A white paper has been published which summarizes and points out for the first time ESD issues in 3D IC integration. In this discussion group we want to exchange the latest R&D results. We will discuss possible ESD design issues but also topics like ESD testing during the 3D integration process.

DG A2: AEC Q100 Meets Industry Council ESD Target Levels
Moderator: Wolfgang Stadler, Intel
wolfgang.stadler@intel.com

Today the main ESD device level qualification methods are ANSI/ESDA/JEDEC JS-001 (HBM) and JS-002 (CDM). In both standards no mandatory threshold levels are defined. The Industry Council for ESD Target Levels set the recommended target robustness values to 1,000 volts for HBM and to 250 volts for CDM which allow safe handling of devices in an ESD protected area. These are typical target values for consumer electronics.

However, those devices are nowadays more and more used in automotive application, and in general in the automotive industry AEC Q-100 applies. The main difference is that target levels are defined in AEC Q-100. These target levels are considerably higher than the values recommended by the Industry Council. The current revision REV-H (2014) defines as accept criteria 2,000 volts HBM and 500 volts CDM (750 volts for corner pins).

We want to discuss how we can bridge the different target levels to allow products for the consumer market where cost-efficiency is a main criterion to be used in automotive applications where zero-fail is a main concern. This discussion includes challenging the target levels in both applications.

DG A3: EOS/ESD in LED Lighting
Moderator: Alessio Griffoni, OSRAM
a.griffoni@osram.com

There is a need in the lighting industry to directly address the understanding of the failure modes and mechanisms induced by EOS/ESD at both component and (sub-) system levels. The true nature of EOS/ESD reliability, especially in light of the rapid advances in the LED lighting industry, requires a comprehensive examination. There are three aspects to address: i) recognition of EOS/ESD failures and their signatures, ii) understanding the nature of component and (sub-) system failures, and iii) estimation of the EOS/ESD technology roadmaps. The main purpose of this DG is to discuss these issues from a variety of perspectives including LED manufacturers, system board designers, and OEMs/ODMs. The target audience spans the range from LED manufacturers to board designers, to OEMs/ODMs because the solution of component and system level EOS/ESD issues requires the effort and the communication from all stages of system development.

IEW 2010, Evangelische Akademie, Tutzing, Germany

Discussion Groups Session B

DG B1: Working with External ESD Consultants, What Can They Do in Times of High Product Pressure?

Moderators: Markus Mergens, QPX
mergens@qpx-europe.com
Stephen Fairbanks, SRF Technologies
stephen@srftechnologies.com

This DG session deals with a discussion on the typical challenges for ESD engineers caused by high product pressure due to limited time and resources. How in your experience do these factors impact the quality of your ESD design and potentially increase the product fail risk? What are measures to mitigate these risks? Moreover, we would like to address this typical work topic in conjunction with making use of external resources. What are the main internal obstacles getting external experts in? How can these consultants support you effectively? What would be optimized working models between internal ESD teams and external resources? Who needs to know what in order to succeed? What advantages do you see in working with consultants? Can they for instance enforce more unpopular ESD protection solutions? Can they more easily work with difficult internal communication channels? What are the main challenges in such a type of cooperation?"

DG B2: Beyond ESD Requirements for Embedded Systems

Moderator: Zhongning Liang, NXP Semiconductors
zhongning.liang@nxp.com

Embedded applications in automotive and autonomous systems require high level of safety and reliability. Additional interactions and understanding of the requirements among the value chains are essential to guarantee the applications working according to requirements during and after the ESD and EMC events. More and more qualification tests (EMC, ESD, surge pulses) are specified at the system level, adding constraints to integrated circuits. These constraints may also impact the business case at the end. How to satisfy all these demands within a single solution? How to balance EMC/interference and ESD in IC design? What is the impact of the different grounding strategies in the packaged product (seal ring, down bonds, etc.)? In this discussion group, we will review the emerging qualification tests for automotive systems and we will debate how to define efficient ESD protection while taking into account all other system requirements.

DG B3: SIG ESD Foundry and IP Vendor Parameters

Moderator: Harald Gossner, Intel, harald.gossner@intel.com

Becoming ESDA WG22 Mobile Communications, the team continues to work on a consolidated recommendation of data exchange and verification tools between IP vendors and IC design which should facilitate a fast and seamless integration of 3rd party IP blocks with ESD and latchup relevance. This is a cross industry activity involving foundries, IP vendors, EDA tool vendors, IC design house, and IDMs. During the meeting along with IEW 2016 it is planned to achieve a final alignment on the crucial aspects of the technical report as they have been identified during previous discussions, workshops and an industry survey. You are invited to join this open meeting and also use the opportunity to provide feedback to the industry survey before IEW (http://bit.ly/1o1kiHe).

Discussion Groups Session C

DG C1: Should Air Discharge CDM Testing Become History?

Moderators: Horst Gieser, Fraunhofer EMFT
horst.gieser@emft.fraunhofer.de
Nathan Jack, Intel
nathan.d.jack@intel.com

It is well known that field-induced CDM (FICDM) testers suffer from a variety of undesirable traits, the most significant of which include zap-to-zap variation, sensitivity to humidity, and difficulty contacting tight pin-to-pin package types. These drawbacks are becoming more bothersome as packages shrink and discharge voltages reduce and design windows close. Contact CDM (CCDM) and Capacitively Coupled Transmission Line Pulsing (CC-TLP) have been proposed as alternative CDM test methods and have demonstrated to eliminate most of these FICDM drawbacks while addressing the CDM-typical failure signatures. CCDM splits into 50 ohm CCDM or "CDM2," and 16 – 25 ohm CCDM. In this discussion group we will debate the pros and cons for future testing standards on CCDM and CC-TLP. Can FICDM, CCDM, and/or CC-TLP co-exist? Should the standards specify a waveform and discharge current but leave it open-ended as to how the pulse is generated, thereby allowing for innovation in CDM tester development?

DG C2: Challenging ESD Device Characterization and ESD Concept Selection in Smart Power Technologies

Moderator: Andreas Rupp, Infineon Technologies
andreas.rupp@infineon.com

On-chip ESD robust design in smart power technologies for industrial and automotive applications must also conform to non-ESD requirements such as ISO7637-2. These requirements often cause trade-off with ESD and hence are challenging for the correct selection of ESD devices and concepts. In this context, many essential questions have been asked which all lead back to the ESD device characterization. Holding voltage smaller than voltage class - is it acceptable for automotive ICs? How can we determine the real clamping voltage of ESD devices concerning voltage overshoots, self-heating, time-out, and ESD pulse shapes? How to avoid hidden ESD weakness in a smart power technology product – can the avoidance be a matter of the scope of ESD characterization? Join the discussion group and bring your own experiences with on-chip ESD design for smart power ICs to the team!

TECHNICAL SESSIONS

Technical Session Chair: Hans Kunz, Texas Instruments, Inc.

This year's IEW technical program consists of three sessions, where peer-reviewed poster presentations are discussed together with the authors and interested colleagues. The authors will introduce their work in a short podium "teaser" presentation prior to the extended interactive discussion with the workshop participants at the posters. This format allows an in-depth exchange of ideas among a diverse audience, in a very informal setting. A wide variety of ESD subjects will be covered, including; ESD cell development challenges, system level design techniques, ESD verification techniques, ESD failure case-studies, and ideas for modeling/simulating both ESD Test systems and ESD cells.

Technical Session A: ESD Testing: Metrology, Trouble-Shooting, and Simulation Techniques/ ESD Verification

A1 Predict the Product Specific CDM-Stress Using Measurement-Based Models of CDM-Discharge Heads

Friedrich zur Nieden, Kai Esmark, Stefan Seidl, Reinhold Gärtner, Infineon Technologies

The introduction of the new CDM-joint standard has an impact on the electrical properties of the tester hardware. The requirements of the waveform during tester verification have changed regarding peak currents and oscilloscope bandwidth. JEDEC- and ESDA-discharge heads do not fulfill the new requirements and a new ESDA/JEDEC-discharge head was designed. For the analysis of the impact of the new hardware on testing results models of CDM-discharge heads are generated using measurement data in frequency domain and a vector fitting algorithm. S-parameters of each discharge head are measured up to 10 GHz in a setup considering influence of the field plane, prober, and positioner. The availability of different models helps to simulate and compare the peak current of a device according to the different CDM-standards. A simple SPICE circuit is used to calculate the discharge of the device capacitance through the discharge head in time domain. Device properties are derived from the dimensions of package and die as well as from the dielectric. CDM-measurement data correlate well with simulated results considering the limited oscilloscope bandwidth. Finally, the influence of the electrical properties of the discharge heads is shown. After the presented results, the new requirements regarding current levels are higher in comparison to the replaced and popular JEDEC-standard.

A2 Simulation and Characterization of Setups for CDM and CC-TLP

Dennis Helmut, Horst Gieser, Heinrich Wolf, Fraunhofer - Research Institution for Modular Solid State Technologies EMFT

The CDM test method shows weaknesses concerning the reproducibility and repeatability of the stress impulses, due to the air discharge and the definition of the tester in the RF-domain. To avoid this uncertainty and in order to increase the repeatability, Gieser and Wolf et al. developed a one pin arc-free method called Capacitively Coupled Transmission Line Pulsing (CC-TLP). Test heads of these methods are compared directly to each other by means of an electromagnetic field simulation. The ability of CDM and CC-TLP to identify differences between pins is shown with statistical significance. Outlook: Different de-embedding techniques are examined for each component in the measurement chain for each method.

A3 CDM Fails Due to On-chip Wiring Inductance

Karl Acker, Robert Haeussler, Heike Schwager, Bernhard Stein, Harald Gossner, Intel Germany

In state-of-the-art full chip, pre silicon ESD verification inductances are not taken into account. However, in this paper a design example is discussed where on-chip wire inductance has been proven to be the main root cause for CDM fails in one of our engineering samples. The design was checked for resistance, distance rules, and local gate protection for sign-off. Due to the low ohmic connection between different VSS bus parts a common VSS can be assumed. Nevertheless, CDM fails stressing a single VDD pin were found. By physical failure analysis, inspection of the layout, detailed analysis of the schematic and analytical calculations of the failure mechanism is traced back to a critical parasitic inductance in the VSS path (in spite of been only detectable when stressing a VDD pin). Significantly reducing the inductance led to a CDM 500 V pass of the device. Other examples are known where package inductances have led to CDM fails. Options and requirements of a pre-silicon ESD verification including the parasitic inductance of the supply rails and package wiring are discussed.

A4 WearOut Effects in HBM Testing

Jian Gao, Theo Smedes, NXP Semiconductors

This work continues the discussion on the topic of "Wearout Effects in ESD Characterization and Testing". In that study, (vf-)TLP, HMM, and CDM results are shown. This work focuses on HBM testing. A wear out impact on ESD testing is confirmed. Since commonly used ESD protections/test structures were selected as examples, the results are directly related to standard qualification work. For ggNMOST, it was found that the HBM wear out dependency is linear and levels off at about 80% of the regular failure level. In a rail based protection structure an unexpected failure was found with a clear wearout contribution.

A5 Verification of SoC Having Pins with Different HBM Targets for ESD Interconnect Checks

V. Sidharth, N. Trivedi, D. Alvarez, Infineon Technologies

Interconnect Checks - Resistance and current density for ESD protection network is an essential part of ESD verification ensuring ESD robustness of SoC. Traditional method of dedicated multiple simulations to verify pins with different HBM targets is time consuming leading to delays with tape outs of SoCs. Proposed methodology enables verification of SoC with pins with different HBM targets in single execution run. Improves results analysis productivity with less uncritical violations as pins with lower HBM targets are not verified with default higher HBM targets. Improves execution time of the checks.

Technical Session B: System Level ESD: Case-Studies, Simulation, and Design Techniques/Compact Modeling of ESD Cells

B1 Display Driver IC's System Level EOS/ESD Failure Case Study with Component Level ESD Test & Current Density Analysis Tool

Sung-Joon Song, Chang-Su Kim, Young-Min Kim, Chan-Hee Jeon, Han-Gu Kim, Samsung Electronics., Ltd.

TV set manufacturers are still struggling with yield loss due to IC failures related to EOS/ESD in TV assembly line, even though TV set manufacturers are requiring IC, module, and set level ESD qualification. Recently a display driver IC failure case related to EOS/ESD in a LCD TV assembly line was reported, and the display driver IC failure was successfully reproduced by newly introduced component level ESD test with IEC-61000-4-2 stress model. Also, the current density analysis tool was used to identify BEOL failure, and it was able to offer the designers a design verification method for the maximum current density of BEOL. The IC manufacturers have difficulty providing ICs robust to system level EOS/ESD stress without knowing the ESD environment of the TV assembly line. In this failure case, system level EOS/ESD performance of IC was possible to predict through the component level ESD test; also it was able to verify IC layout design though the current density analysis tool for the BEOL on-chip system level solution.

B2 Ideas to Make the SEED Approach More Practically Usable for System Designers

Michael Ammer, Infineon Technologies

The SEED approach was developed to enhance the predictability of ESD withstand levels according to ISO10605 tests. But how applicable is this approach in the development of electronic systems? The Industry Council on ESD Target Levels proposes the use of TLP data to characterize the transient behavior of the components. But no semiconductor manufacturer provides this data to its customer, mainly due to intellectual property reasons. You could characterize the components in ESD time domain on your own. This takes much effort in terms of equipment cost, measurement knowledge, and time. A better method is to provide some additional parameters in the device datasheet, e.g. not only breakdown voltage but also clamping voltage at a certain current in case of TVS diodes. If SEED is not easy to use for everybody then only a few persons will use it. Imagine you are a system designer and should do additional ESD considerations which means a lot of additional effort. Would you do an ESD check? There will be a proposal for additional parameters to integrate into datasheets to make the SEED approach easy to use.

B3 Impact of ESD on an Electrical System-ESDA WG26 Results

Fabien Escudié, Fabrice Caignet, LAAS/CNRS; Robert Ashton, ON Semiconductor; Davis Jordan, Diodes, Inc.; Yen-Yi Lin, EMC, Guido Notermans, NXP Semiconductors; Benjamin Orr, Harald Gossner, Intel; Mirko Scholz, imec

The 2010 Industry Council white paper on system level ESD addresses the need for standardized models which can be used in system level ESD simulation. These models should cover the high current behavior of IC I/O pins, supply pins, and discrete components during ESD timescales to the point of failure. The goal is to enable a seamless simulation environment where standard PCB or circuit simulation tools can be applied towards system level ESD simulation. The ESDA standard working group 26: "Models for System Level Simulations" is currently working on a technical report which defines the construction of such models from mea-

B3 Impact of ESD on an Electrical System-ESDA WG26 Results-continued

surement to design flow implementation. In this document, a minimum set of parameters are outlined which describe the IV behavior of IC pins as well as their hard failure thresholds. Using these parameters, IC models are proposed with the intent to cover both quasi-static and transient simulations. Categories of model accuracy and coverage will be defined. To validate the technical report a set of experiments are underway. Seven labs have volunteered to evaluate the methodology (from model extraction to simulation results) in a round-robin approach. The method is tested on three disparate systems covering digital, automotive, and high speed communications link applications. Results and comparisons with the respective measurements are presented.

B4. Evaluation of ESD Stress Application Methods for Identification of Soft Failure Mechanisms

Sebastian Koch, Harald Gossner, Intel; Horst Gieser, Fraunhofer-Einrichtung für Mikrosystemeund; Linus Maurer, Universität der Bundeswehr München

The objective of this work is to identify failure mechanisms of soft failures in mobile devices early in the product life cycle. Different methods of applying system level ESD stress are used to trigger and identify different soft failure modes. A transmission line pulse setup was used to directly contact and inject ESD stress on USB 3.0 data lines to investigate the influence of pulse parameters. Different failure modes could be identified and their dependence on the state of USB data transmission has been investigated. IEC 61000-4-2 stress induced the same failure modes. By use of a magnetic field probe, different entry paths for field coupling were revealed on the device under test. Observation of the DUT's power domains is used to discern the root cause of failures, e.g. to distinguish between supply noise or transient latch-up related failures. This includes monitoring of voltage droops or overshoots as well as current flow to the device from the PMU and decoupling capacitors. Measurements are supported by simulation of the package parasitics and intentional injection of power supply noise.

B5 Validation of Compact Modeling Simulation of Snapback-Based ESD Protection Using Circuit Test Cases

Efraim Aharoni, Avi Parvin, Israel Rotstein, Yosef Raskin, TowerJazz

Few circuit test-cases like soft-pull down ESD NMOS transistor were used to develop, debug, and validate snap-back based ESD clamping simulation in protection schemes. The simulator was based on VerlilogA piecewise-linear compact modeling and TLP characterization of stand-alone ESD transistors at various gate voltages (fed to the simulator as triggering conditions). The simulation results were compared to TLP measurements on actual circuits put on silicon. Agreement between the simulation and measurements helped in validation. On the other hand, disagreements are important aids for debugging and improving the simulation accuracy and relevance.

Technical Session C: ESD Cell Development: Novel Requirements and Technology Challenges

C1: Specific Considerations for Boosted RC Rail Clamp ESD Protection Design

Efraim Aharoni, Avi Parvin, Israel Rotstein, Yosef Raskin, TowerJazz

This work describes the efforts to design a high ESD rating (HBM rating>4kV) I/O library for 1.8V only process, tolerant to input over-voltage of up to 4V. Snap-back based ESD protection choice is not relevant due to the poor ESD window. Boosted (active) RC rail clamp was used with cascaded transistors in bigFet, inverters, and other places exposed to the over-voltage. BigFet gate voltage was boosted above the nominal 1.8V to reduce the IC area consumed for ESD protection. This presentation is focused in challenges like measurements and modeling of the nominal transistors for gate voltages above Vdd, as well as the reliability considerations. Pulsed-DC characterization of the transistors was utilized for SPICE models beyond Vdd, preventing devices degradation during measurements. Based on this work, formal nominal devices pcells for boosted bigFET, with special SPICE models, were released in TowerJazz ESD PDK. They can be used in cases of harsh ESD design specifications and need to save IC area consumed by the RC rail clamp ESD protection.

C2: Dynamically Boosted Substrate Power Clamp for Reduced Leakage and Improved Speed

S. Radhakrishnan, Jean Jimenez, ST Microelectronics Pvt. Ltd.; M. Jagadesh Kumar, Indian Institute of Technology

The objective of this paper is to come up with a new supply clamp which reduces the DC leakage current and improved CDM and HBM performance at the reduced cost. Typically power clamps are realized using high threshold voltage (VT) transistors which cause additional cost to the customer due to the extra mask requirement but using the regular standard VT transistor increases the leakage current. The second problem with the state-of-the-art power supply clamp is the robustness towards the fast charging transients like CDM events. The proposed supply clamp is realized using standard VT transistors. To reduce the leakage current and improve the turn-on speed, the substrate is boosted to turn-on the parasitic BJT through an additional inverter. Hence the power clamp works in Forward Body Bias (FBB) mode during an ESD event and works as standard device with its substrate connected to ground during normal operation. To strengthen the claims, we have included the SPICE simulation results for HBM/CDM standards. Non-isothermal TCAD simulations are also performed to determine the operating mechanisms of BJT. The proposed clamp is qualified in silicon for 2KV HBM, 500V CDM. We have also included the TLP results.

C3: Development of Area-Efficient High-Voltage Bi-Directional ESD Protection for Automotive Applications

Carol Rouying Zhan, Changsoo Hong, Kurt Neugebauer, Jean-Philippe Laine, Patrice Besse, Freescale Semiconductor

Automotive ICs require high ESD robustness. In addition to a 2KV HBM/500V CDM compliance level for all the pins on-chip, a subset of pins with direct contact to external environment must sustain system-level IEC and/or ISO "gun" stress (IEC 61000-4-2, ISO-10605). As a result, ESD protection structures could take significant die area. This work presents two techniques to build area-efficient HV bi-directional ESD protection for automotive applications on Smart Power technologies. 1) Asymmetrical device architecture to improve current capability. With asymmetrical device architecture, 120 mA/µm current capability, one of the highest reported in literatures, was achieved. This translates to excellent area-efficiency. 2) Share stack among multiple pins to reduce die area. With part of ESD protection shared among multiple pins, die area of ESD clamps can be significantly reduced without impacting targeted parameters. The proposed ESD protection has been validated on Freescale's 0.18 µm technology. In addition to excellent TLP results, it passed 10KV IEC 61000-4-2 (RC=330 ohm,150 pF) with Le=300 µm without external components. It is also achieved similar robustness with more rigorous ISO-10605 test (RC=330 ohm, 330 pF). It meets EMC DPI (direct power injection) requirement of 35 dBm per IEC 62132-4. The proposed ESD protection has been successfully integrated in automotive ICs.

C4: Challenges for ESD Solutions in Germanium-Based Technologies

Roman Boschke, Guido Groeseneken, KU Leuven, imec; Geert Hellings, Shih-Hung Chen, Mirko Scholz, Dimitri Linten, Aaron Thean, imec

Germanium is a high mobility material and a candidate channel material for future scaled FinFETs. The high contact resistance on n+ doped Ge is an issue for further implementation. Strong Fermi-level pinning and limited n-type dopant activation in Ge causes a Schottky barrier to be present. This will have an impact on the ESD performance of Ge FinFET gated diodes. This work presents a study of this issue through measurements on test structures with variable contact area on both terminals of Ge diodes. Integration of Ge on Si creates a Ge/Si heterostructure, which can have a profound impact on the electrical characteristics. Previous studies on planar STI diodes with Ge/Si heterostructure showed different behavior, depending on whether the n+ or p+ terminal is fabricated in Ge. It is fundamental to understand the impact of such Ge/Si interface to gain further understanding. This work presents a detailed study of diodes with Ge/Si heterostructure.

Technical Session C: ESD Cell Development: Novel Requirements and Technology Challenges-continued

C5 Impact of Wafer Thinning on ESD Protection Devices in 3D Integrated Systems

Mirko Scholz, Adrian Chasin, Dimitri Linten, Geert VanderPlas, Eric Beyne, imec

3D integration is one promising option for further effective scaling of integrated circuits (IC). It enables higher integration density, more heterogeneous integration, and thus more functionality per footprint. To increase further the interconnect density, through-silicon via (TSV) sizes are scaled from currently 10 µm to below 1µm in the coming years. The aspect ratio during TSV etching requires a drastic reduction of the wafer thickness down to 5µm to enable these next generation TSV. We will show in this poster the impact of this thinning process on the performance of typical ESD protection devices like diodes and SCR-based clamps.

C6 Simulation on Rotated STI Diodes in Advanced Bulk FinFET Technology

Shih-Hung Chen, Dimitri Linten, Geert Hellings, Mirko Scholz, Roman Boschke, Aaron Thean, imec

In CMOS scaling roadmap, bulk FinFET is the mainstream technology for sub-20nm nodes. In previous work, two types of ESD protection diodes are studied. The results show ~50% reduction of parasitic capacitance of the STI diode compared to the gated diode, makes the STI diode a preferred diode type for high frequency applications. The higher Ron of the STI diode can be reduced by an alternative layout style. Instead of separating the anode and cathode of a diode along the same fin with an STI cut (of length D), a rotated STI diode structure is proposed. The anode and cathode are separated by 1 or more fin pitches in order to prevent the anode and cathode fins to shorten by the following epitaxial Si re-growth or local interconnect processes. However, the further optimizations on fin numbers of each anode and cathode node were not studied. In this work, the optimizations of the rotated STI diodes are done by TCAD simulations. The fin numbers of the anode and cathode have strong impacts on ESD diode performance of It2/W layout and Ron.

IEW 2010, Evangelische Akademie, Tutzing, Germany

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Monday, May 16, 2016

4:00 PM-7:00 PM	**Registration:** Pick up badges and handouts.
4:00 PM-7:00 PM	**Hotel check-in:** Get room assignment & room key.
7:00 PM-9:00 PM	Bavarian Evening: IEW welcomes travelers from abroad and local guests with a colorful program of Bavarian traditions ranging from an archetype of communication 'Jodeln' to a particular form of dancing 'Schuhplattln'. Join and meet your friends and peers in a relaxed atmosphere.

Tuesday, May 17, 2016

8:00 AM-11:45 AM	**Registration:** Pick up badges and handouts.
7:30 AM-4:30 PM	**Hotel check-in:** Get room assignment & room key.
7:30 AM-9:30 AM	**Breakfast**
10:00 AM-10:15 AM	Welcome
10:15 AM-11:00 AM	**Keynote: Robustness Challenges for Technologies 28nm and below in Automotive Environment,** *Jürgen Weyer, NXP Semiconductors*
11:00 AM-11:45 AM	**Invited Talk 1: ESD Protection Devices and Technologies: Recent Advances and Trends,** *Werner Simbürger, Infineon*
11:45 AM-12:45 PM	**Lunch**

12:45 PM-1:15 PM

Technical Session A: ESD Testing: Metrology, Trouble-Shooting and Simulation Techniques/ ESD Verification

A1 Predict the Product Specific CDM-Stress Using Measurement-Based Models of CDM-Discharge Heads
Friedrich zur Nieden, Kai Esmark, Stefan Seidl, Reinhold Gärtner, Infineon Technologies

A2 Simulation and Characterization of Setups for CDM and CC-TLP
Dennis Helmut, Horst Gieser, Heinrich Wolf, Fraunhofer - Research Institution for Modular Solid State Technologies EMFT

A3 CDM Fails Due to On-Chip Wiring Inductance
Karl Acker, Robert Haeussler, Heike Schwager, Bernhard Stein, Harald Gossner, Intel

A4 WearOut Effects in HBM Testing
Jian Gao, Theo Smedes, NXP Semiconductors

A5 Verification of SoC Having Pins with Different HBM Targets for ESD Interconnect Checks
V. Sidharth, N. Trivedi, D. Alvarez, Infineon Technologies

1:15 PM-2:30 PM	**Poster Discussion Session A**
2:30 PM-2:40 PM	**Break**
2:40 PM-2:45 PM	Announcements
2:45 PM-4:05 PM	**Seminar 1: Analysis of ESD Testing Induced Failures** *Yong-Fen Hsieh, Materials Analysis Technology, Inc. (MA-tek)*

Tuesday, May 17, 2016 continued

4:05 PM-4:35 PM	**Technical Session B: System Level ESD: Case-Studies, Simulation and Design Techniques/Compact Modeling of ESD Cells**

B1 Display Driver IC's System Level EOS/ESD Failure Case Study with Component Level ESD Test & Current Density Analysis Tool

Sung-Joon Song, Chang-Su Kim, Young-Min Kim, Chan-Hee Jeon, Han-Gu Kim, Samsung Electronics., Ltd.

B2 Ideas to Make the SEED Approach more Practically Usable for System Designers

Michael Ammer, Infineon Technologies

B3 Impact of ESD on an Electrical System - ESDA WG26 Results

Fabien Escudié, Fabrice Caignet, LAAS/CNRS; Robert Ashton, ON Semiconductor; Davis Jordan, Diodes, Inc.; Yen-Yi Lin, EMC, Guido Notermans, NXP Semicinductors; Benjamin Orr, Harald Gossner, Intel; Mirko Scholz. imec

B4. Evaluation of ESD Stress Application Methods for Identification of Soft Failure Mechanisms

Sebastian Koch, Harald Gossner, Intel; Horst Gieser, Fraunhofer-Einrichtung für Mikrosystemeund; Linus Maurer, Universität der Bundeswehr München

B5 Validation of Compact Modeling Simulation of Snapback-Based ESD Protection Using Circuit Test Cases

Efraim Aharoni, Avi Parvin, Israel Rotstein, Yosef Raskin, TowerJazz

4:35 PM-4:45 PM	**Break**
4:45 PM-6:00 PM	**Poster Discussion Session B**
6:00 PM-7:00 PM	**Dinner**
7:00 PM-8:00 PM	**Discussion Group Session A: Parallel Groups**

DG A1: ESD Reliability in 3D Integration Technologies
DG A2: AEC Q100 Meets Industry Council ESD Target Levels
DG A3: EOS/ESD in LED Lighting

8:00 PM-9:00 PM	**Special Event:** **Development of Human Communication Skills -The Perspective of an Anthropologist** *Prof Vasu Duvvury*

Human-Machine-Interaction for Advanced Driver Assistance Systems (ADAS) and Highly Automated Vehicles (HAV) *Prof Berthold Färber, University of Armed Forces, Munich*

Wednesday, May 18, 2016

7:00 AM-8:00 AM	**Breakfast**
8:00 AM-8:05 AM	Announcements
8:05 AM-8:20 AM	Report on DG Sessions
8:20 AM-9:40 AM	**Seminar 2:** **Advances in Contact CDM and CC-TLP Methods**
	Nathan Jack Intel Corporation; Horst Gieser, Fraunhofer EMFT
9:40 AM-9:50 AM	**Group Photo**
9:50 AM-10:00 AM	**Break**
10:00 AM-10:45 AM	**Invited Talk 2:** **Road to Self Driving Cars – View of a Semiconductor Supplier**
	Hans Adlkofer, Infineon Automotive System
10:45 AM-11:30 AM	**Invited Talk 3:** **View from a Leading Car Manufacturer or System Supplier to Semiconductor Requirements Supporting Autonomous Driving** *Ulrich Abelein, AUDI*
11:30 AM-11:50 AM	**Overview on USCAR and ESDA Joint Activities** *Reinhold Gärtner, Infineon Technologies*
11:50 AM-12:50 PM	**Lunch**
12:50 PM-5:00 PM	**Open Time**
5:00 PM-6:00 PM	**Discussion Group Session B: Parallel Groups**

DG B1: Working with External ESD Consultants–What Can They Do in Times of High Product Pressure?
DG B2: Beyond ESD Requirements for Embedded Systems
DG B3: SIG ESD Foundry and IP Vendor Parameters

6:00 PM-7:00 PM	**Dinner**
7:00 PM-8:00 PM	**Discussion Group Session C: Parallel Groups**

DG C1: Should Air Discharge CDM Testing Become History?
DG C2: Challenging ESD Device Characterization and ESD Concept Selection in Smart Power Technologies

Thursday, May 19, 2016

7:00 AM-8:00 AM	Breakfast
8:00 AM-8:05 AM	Announcements
8:05 AM-8:35 AM	Report on DG Sessions
8:35 AM-8:50 AM	Industry Council Report
8:50 AM-9:00 AM	Major Changes in Latch-up Standard – Outlook on JESD78F, *Wolfgang Stadler, Intel*
9:00 AM-9:45 AM	**Invited Talk 4:** **Electrical Overstress (EOS) – Developing a Common Language and Understanding,** *Brett Carn, Harald Gossner, Intel*
9:45 AM-10:00 AM	Break

10:00 AM-10:35 AM	**Technical Session C: ESD Cell Development: Novel Requirements and Technology Challenges**

C1: Specific Considerations for Boosted RC Rail Clamp ESD Protection Design
Efraim Aharoni, Avi Parvin, Israel Rotstein, Yosef Raskin, TowerJazz

C2: Dynamically Boosted Substrate Power Clamp for Reduced Leakage and Improved Speed
S. Radhakrishnan, Jean Jimenez, ST Microelectronics Pvt Ltd.; M. Jagadesh Kumar, Indian Institute of Technology

C3: Development of Area-Efficient High-Voltage Bi-Directional ESD Protection for Automotive Applications
Carol Rouying Zhan, Changsoo Hong, Kurt Neugebauer, Jean-Philippe Laine, Patrice Besse, Freescale Semiconductor

C4: Challenges for ESD Solutions in Germanium-Based Technologies
Roman Boschke, Guido Groeseneken, KU Leuven, and imec; Geert Hellings, Shih-Hung Chen, Mirko Scholz, Dimitri Linten, Aaron Thean, imec

C5 Impact of Wafer Thinning on ESD Protection Devices in 3D Integrated Systems
Mirko Scholz, Adrian Chasin, Dimitri Linten, Geert VanderPlas, Eric Beyne, imec

C6 Simulation on Rotated STI Diodes in Advanced Bulk FinFET Technology
Shih-Hung Chen, Dimitri Linten, Geert Hellings, Mirko Scholz, Roman Boschke, Aaron Thean, imec

10:35 AM-12:05 PM	**Poster Discussion Session C**
12:05 PM-1:05 PM	Lunch
1:05 PM-2:25 PM	**Seminar 3:** **EOS/ESD Challenges in LED Lighting** *Alessio Griffoni, OSRAM*
2:25 PM-2:35 PM	Break
2:35 PM-3:55 PM	**Seminar 4:** **The Design Engineer: Weak link or Warrior in the ESD Battle?** *Ginger Hansel, Dangelmayer Associates*
3:55 PM-4:10 PM	2017 Announcements and Closing
7:00 PM-9:00 PM	Farewell: After a fully-loaded program the farewell party on Thursday night is the opportunity to exchange final thoughts and wrap up while enjoying Bavarian beverages.

IEW 2015 group photo

Travel Arrangements & Accommodations

WORKSHOP VENUE
Evangelische Akademie • Schlossstrasse 2 • 82327 Tutzing
Telefon: 08158 2510 Telefax: 08158 996444
Internet: http://www.ev-akademie-tutzing.de

ARRIVAL AT EVANGELISCHE AKADEMIE
The workshop will begin Tuesday, May 17th: 10:00 a.m.
Monday evening registration hours are scheduled from 4:00 PM-7:00 PM;
Tuesday registration hours begin at 8:00 AM

TRANSPORTATION
Tutzing, Germany is located about 40 km south of Munich at the western shore of Lake Starnberger See.

From Munich by Rail
From Munich International Airport take metro (S-Bahn) S1 or S8 to main station (Hauptbahnhof). Change trains there to S6 heading to Tutzing. Leave S6 at the final destination of Tutzing. It takes about 10 minutes to walk from Tutzing station to the Evangelische Akademie via Bahnhofstrasse, Hallberger Allee and Hauptstrasse to Schlossstrasse. Tickets for the S-Bahn can be bought at the information counter of the airport in Terminal 1 next to the escalators to S-Bahn.

It takes about 1 hour 30 minutes by train from the airport to Tutzing.

Train schedules http://www.mvv-muenchen.de/en/home/index.html

From Munich by Car
Exit the airport on motorway A92 heading Munich (München). At junction 4 München/Salzburg take A9 to Munich (München). At the end of the motorway (exit 76) turn right to ring road West (Mittlerer Ring West) following the signs to Garmisch-P. At junction to A95 enter motorway A95 in the direction of Garmisch-Partenkirchen. Take exit to Starnberg. In Starnberg take the B2 federal road towards Weilheim with destination Traubing. In Traubing you turn left and follow the signs guiding you to Tutzing.

It takes about 1 hour 15 minutes by car from the airport to Tutzing.

Car rental: http://www.munich-airport.de/en/consumer/anab/mietwagen/index.jsp

IEW ACCOMMODATIONS
IEW attendees pay a package fee which covers the workshop registration, three nights of lodging, and meals. Attendees are welcome to bring guests for an additional package fee covering the three nights of lodging and meals. Please see the registration form for full details.

The Evangelische Akademie Tutzing offers single and double guest rooms. Some of the rooms are located in the old castle wing and some located in the modern guest house. You can enjoy a wonderful view over Lake Starnberger See and the spacious park surrounding the building. All rooms offer private shower, WC and telephone. The arrangements in some of the guest rooms have been adjusted to the particular needs of handicapped guests.

● No reductions to the package fee will be made for partial stays or unused meals.
● Smoking is permitted outdoors only.
● Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or email to info@esda.org
● A list of restaurants near the Academy can be found at http://www.tutzing24.de/tourismus/branche.php?a=gastronomie

RESPONSIBILITIES OF ATTENDEES
You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IEW!

In keeping with the relaxed and informal atmosphere of the workshop, we ask that attendees not overtly solicit, promote, or attempt to sell a commercial product or service at the workshop. On the other hand, we strongly encourage making business acquaintances and arranging meetings to be held after the workshop.

FOR YOUR VISIT
May usually has nice weather with warm spring days. Warm clothing is recommended when walking in the evening since the nights can be a bit chilly. There are trails at the lake and in the surrounding hills. Sturdy shoes are useful for walking the surrounding areas. Comfortable, informal dress is encouraged during the conference.

International ESD Workshop Registration

May 17-19, 2016 Evangelische Akademie, Tutzing, Germany
Workshop registration includes a room reservation and provided meals

Register Online at www.esda.org/events/iew/

Registration Fee $2,195

Discount before April 1st: members $1,795 / non-members $1,995

The registration fee includes full workshop attendance and handout materials, three nights' lodging (Mon-Wed), plus 9 meals (Tuesday Breakfast -Thursday Dinner), as well as morning and afternoon breaks. Attendees who wish to stay Thursday night will be charged an additional $130 USD.

Note: Based on room availability or additional Thursday night stay requests the IEW management committee may place attendees at an alternate hotel near the Evangelische Akademie.

Cancellation & refund requests will be considered if received in writing no later than April 1, 2016, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Register 5 or more people from one company at the same time and save $100 per person Please contact the EOS/ESD Association, Inc. prior to registering.	Students wishing to apply for reduced registration Please contact the EOS/ESD Association, Inc. prior to registering.

The German ESD FORUM e.V. supports the attendance of students. Students may apply for a 1.000 EUR grant for IEW attendance fee from the German ESD Forum (info@esdforum.de) until March 21, 2016. The application should include the topic of the student's work and the technical presentation(s) intended for the IEW. Selected students will be informed before the early registration deadline (April 1, 2016).

IEW Gold Sponsorship bundles:

Option 1: Register eight attendees from one company at the same time for $12,000

Option 2: Register ten attendees from one company at the same time for $15,000

Please contact the EOS/ESD Association, Inc. prior to registering. *Save $695 per person.*

International ESD Workshop Registration Form

Workshop registration includes a room reservation Mon-Wed nights and provided meals

Attendee: _____

Company: _____

Address: _____

City: _____ State: _____ Zip: _____ Country: _____

Phone: _____ E-mail: _____

Address is: *(Please check one)* ☐ home or ☐ office
☐ Please check here if you would like a printed set of notes.　　　☐ Check if, under the Americans with Disabilities Act, you require any auxiliary aids or services.

•Please List Your Guests: Adults (Name) _____
Guests staying in the room of a registered attendee will be charged $550 USD per person. Guest fees are payable to ESDA. Guests will be charged for full stay, no partial stay is allowed. For accomodations including children please contact ESDA for more information.

•Please indicate any special dietary needs. _____

Arrival: Date _____ Time _____ • Departure: Date _____ Time _____

Registration Fee $2,195

Discount before April 1st: members $1,795 / non-members $1,995

The registration fee includes full workshop attendance and handout materials, three nights' lodging (Mon-Wed), plus 9 meals (Tuesday Breakfast -Thursday Dinner), as well as morning and afternoon breaks.
Attendees who wish to stay Thursday night will be charged an additional $130 USD.
　　　☐ Please check if you will be staying Thursday night

Cancellation & refund requests will be considered if received in writing no later than April 1st, 2016, and are subject to a $50 fee.
Any other approved dispositions will also be assessed a $50 fee.

Method of Payment

☐ Check　　Only U.S. currency, checks drawn on a U.S. bank that is a member of the U.S. Federal Reserve will be accepted.

Credit Card *(check one)* ☐ AMEX® ☐ Visa® ☐ MasterCard® ☐ Discover®

Card Number: _____

Exp. Date: _____ Security Code: _____

Name on Card: _____ Signature: _____

Billing Address: _____

Total Enclosed $ _____
Make checks payable to: EOS/ESD Association, Inc.
Purchase orders not accepted for registration

The EOS/ESD Association accepts payment in the form of a wire transfer, a $15 wire fee must be ADDED to the total fees due. (You also have to ensure that all fees from your bank and any transfer banks are also ADDED to the amount you transmit.)

Discussion Groups

I am interested in the following discussion group(s)
Choose one from each group;

Group A　　　Group B　　　Group C
☐ DG A.1　　☐ DG B.1　　☐ DG C.1
☐ DG A.2　　☐ DG B.2　　☐ DG C.2
☐ DG A.3　　☐ DG B.3

Special Interest Groups

Would you like to form a new SIG? ☐ Yes　☐ No
If yes, what is the proposed topic for your group?

_____

Posters

Will you be bringing a poster to the open poster session? ☐ Yes　☐ No
If yes, what is the title of your poster? _____